A High-Speed, Multi-Channel Data Acquisition System

Dexter Malley, Bob Brown, Edgar Kennedy, Roger Meredith, and Steve Stanic

Naval Research Laboratory, Code 7184, Stennis Space Center, Ms. 39529

Abstract. The Naval Research Lab is currently conducting research programs in MCM detections and classifications using both low and high frequency acoustics. These include target detections, target imaging, proud and buried target detections and classifications using structural clues. To determine the limitations that a fluctuating environment places on these target detection methods, a data acquisition system was developed. The data acquisition system consists of multi-channel, high-speed A/D's with remote, variable gain control, and FPGA technology. Each A/D is synchronously sampled at a rate of 1 MHz and using time-division multiplexing techniques, is sent down an optical fiber at 1.3 Gbps. The sampled data is then separated back to its original channel and recovered back to an analog signal along with the original clock. Precision filters and high speed transient recorders utilizing fast CAMAC crate controllers are then employed to sample, simultaneously, all data channels with sample rates up to 3Msps. Acoustic and environmental real-time software were developed using National Instruments Labview to generate the CW source signals that went from 10 kHz to 200 kHz, monitor acquired data, and control sample and repetition rates.

INTRODUCTION

In June 2003, the Naval Research Laboratory conducted a series of vary-shallow-water, broadband coherence experiments. These measurements used large aperture vertical and horizontal low-frequency receiving arrays, a pair of multi-channel, high frequency receiving arrays, and a multi channel buried hydrophone array. Since it was necessary to record data simultaneously from many of these channels, a new digital multi-channel data acquisition system was designed and built. This system acquired data from 44 channels and multiplexed this data onto one optical fiber. This data was then sent to an instrumentation van located on shore. A complete description of the measurements, program objectives, and at-sea experimental configuration is given in [1]. This paper will describe the signal generation and the multi-channel data acquisition system, and control functions.

System Description

An overview of the complete system is shown in Figure 1. The system is divided

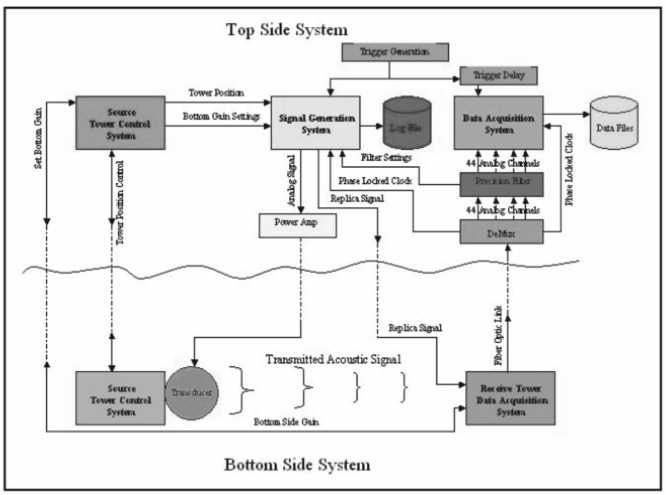

FIGURE 1. System Overview

into two distinct sections: acoustic signal generation / data acquisition, and tower control (position and amplifier gain). Each of these sections include both a topside and a bottomside component. The topside signal generation is illustrated in Figure 2.

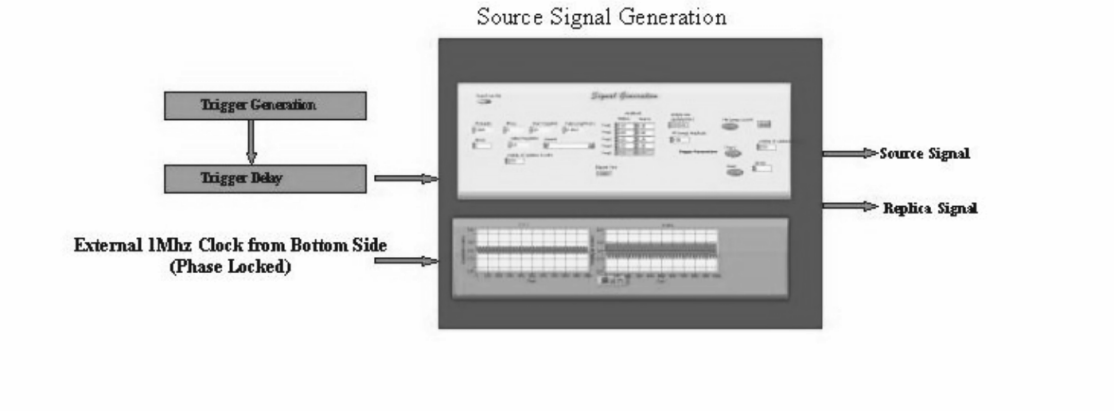

FIGURE 2. Topside Signal Generation

A 10 MHz master clock signal is generated in the bottomside receive electronics and transmitted to the topside signal generation system via a fiber optic link. This clock is divided down to generate a 1 Hz trigger and the 1 MHz sample clock. Acoustic signal generation is accomplished using a National Instruments PC-MIO 16 Multifunction I/O Board controlled by a PC with a 1 GHz processor. User Interface software is written in National Instruments LabView, and provides the capability of generating high-frequency CW signals with a user specified amplitude and pulse length. It was also used to generate a broadband, low-frequency, digital signal from a user supplied data file. During these measurements, two signals are generated: the source signal which is transmitted via the source transducer, and a replica signal which

is transmitted through all of the receive electronics to quantify the system electronic noise and phase stability.

Bottomside Electronics

The bottomside system was designed to acquire 44 channels of real-time data. Each individual data channel was synchronously digitized at 1 MHz with addressable, programmable gain up to 58 dB. The channels are multiplexed down to 11 channels and then serialized into a single bit stream. This bit stream is then transmitted via optical fiber to a receive station located onshore. Once received, the bit stream is then deserialized back to 11 channels and demultiplexed back to 44 channels. The original sampling clock is also retrieved from the incoming bit stream. Finally, each of the 44 individual digital channels is passed to digital-to-analog (D/A) converters, which restores the analog signals to their original form. A simple system block is shown in Figure 3.

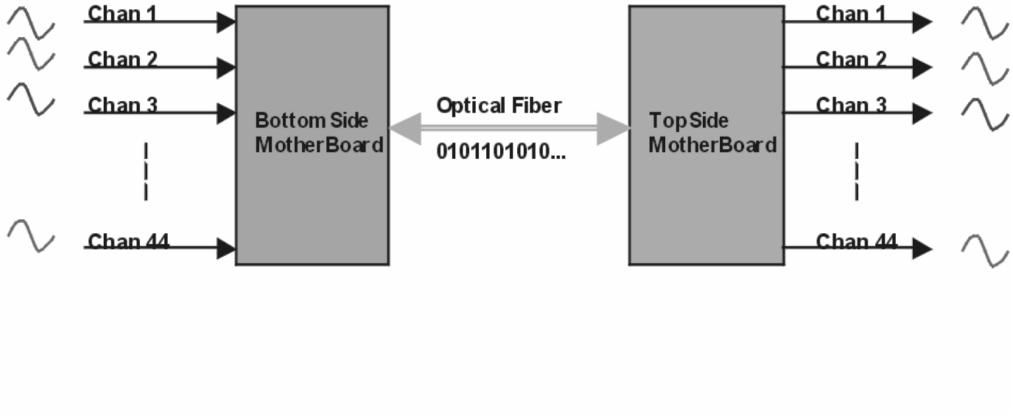

Figure 3. System Block Diagram

The electronics for the bottomside consists of 2 major parts, the A/D boards and the bottomside motherboard. A block diagram of the A/D board is seen in Fig. 4.

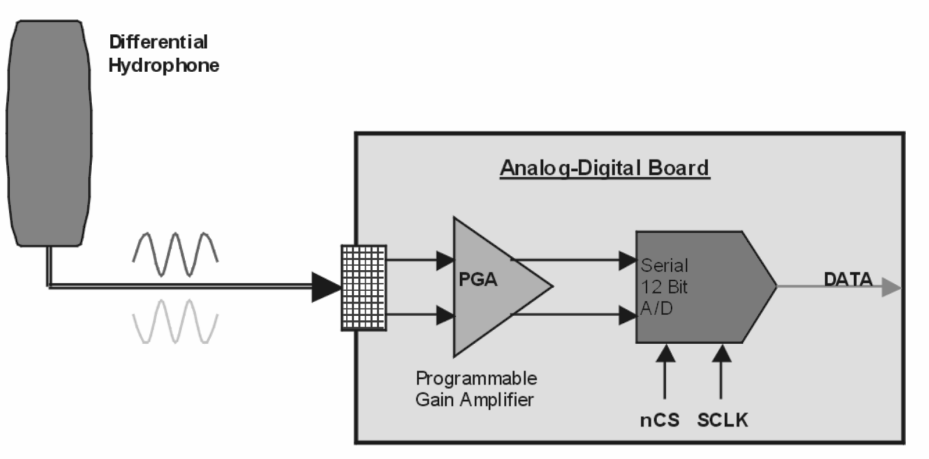

FIGURE 4. A/D Board

The output of the hydrophone goes to a Programmable Gain Amplifier (PGA) which has selectable gain from 0 to 58 dB in 6 dB increments. Each module has an 8-bit address and a 4-bit gain register. A PC computer topside writes down individual gain settings for each A/D board. The differential signal from the PGA is then passed to an anti-alias filter, and converted to a digital stream using a 12-bit A/D converter. The conversion and timing are controlled using chip select, nCS, commonly known as a framing bit, and a serial clock, SCLK.

The final part of the bottomside electronics is the motherboard. As shown in Figure 5, the bottomside motherboard is made up of 3 major components: a Field-Programmable Gate Array (FPGA), a serializer, and a fiber optic transmitter. The first component, the FPGA, was used mainly because they are reprogrammable, flexible, low cost, and low power. Because FPGA's are reprogrammable, it removes the non-recurring engineering cost from prototyping and testing new designs. Once a design is created, simulation routines can be done on a PC to debug any hardware or timing issues. Lastly, a FPGA allows the platform to be reconfigured for future designs.

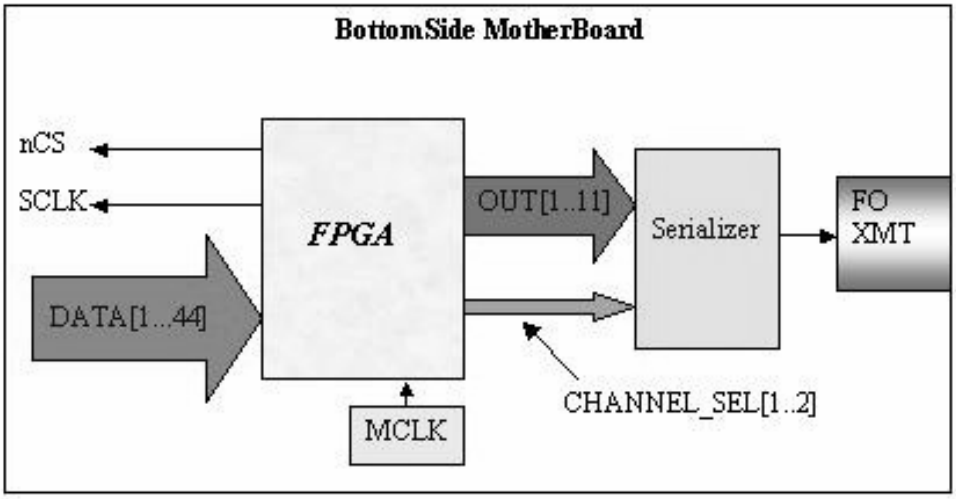

FIGURE 5. Bottomside Motherboard

The FPGA for this project provides three major functions which are clock dividing, multiplexing and counting. As stated above, the A/D modules need two timing and control signals, SCLK and nCS. These two signals are created in and fanout from the FPGA. In this case, SCLK is 18 MHz. This signal is generated by taking the free-running master clock, MCLK, which is 72 MHz and dividing it by four. To get the framing or sync signal, nCS, the SCLK is fed into a counter. For every 16th clock pulse of SCLK, nCS will go high for 1 clock pulse. This clock pulse initiates the synchronous sampling for all of the A/D's.

The digital data from the 44 A/D modules are routed to individual input pins on the FPGA. Inside the FPGA, the digital data from each A/D channel is input into a 4 channel, 11-bit wide multiplexer. These 44 data channels are separated into 4 groups of eleven as seen in Figure 6. Each group is sampled or switched into the output of the multiplexer at a rate of MCLK (72 MHz) or 4 times the frequency of SCLK.

The CHANNEL_SEL[1..2] is a binary 2-bit counter that repeatedly counts from 1 to 4 to sequentially switch the groups.

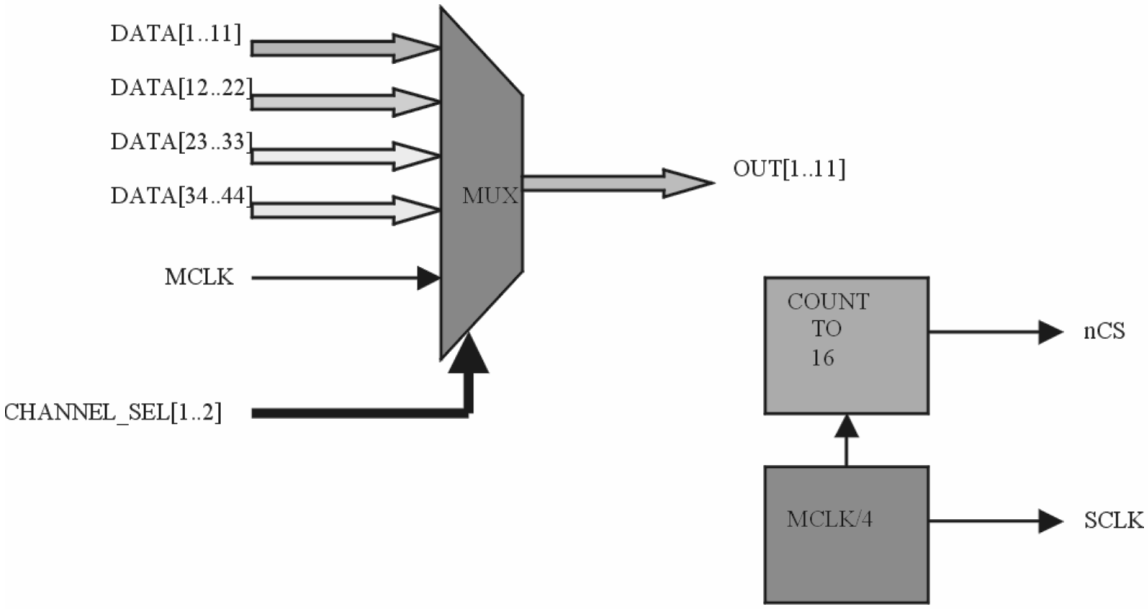

FIGURE 6. FPGA Multiplexer and Clocking

The next major component of the bottomside motherboard is the serializer. The serializer that was used is a 16-to-1, meaning it serializes 16 inputs into 1 output. For this application, only 13 inputs will be used; 11 from the output of the multiplexer and 2 from CHANNEL_SEL. The 3 remaining unused inputs are tied low. Using the serializer has several advantages. One major advantage is that the serializer uses 8B/10B encoding which guarantees at least one transition for every character which

maximizes a synchronization sequence [2]. Next, the serializer's counterpart, the deserializer, generates the original master clock utilizing an internal phase-lock loop, PLL. Because of the high-speed signal, the serializer outputs a low-voltage, differential signal, LVDS. This helps minimize crosstalk and noise throughout the circuitry. The serializer transmits the data and clock bits (16+2 bits) at 18 times the MCLK frequency. This is calculated by the following:

MCLK * (16 inputs + 1 start bit + 1 stop bit) = 72 MHz * 18 = 1.296 Gbps. [3]

The final component is the fiber optic transmitter. The transmitter accepts the differential output of the serializer, converts it to light and transmits the data through a single-mode fiber to the receiving topside motherboard located onshore.

Topside Electronics

Like the bottomside, the topside motherboard is made up of similar components: an FPGA, deserializer, and a fiber optic receiver. The fiber optic receiver takes the optical data where is it converted again to a low-voltage, differential signal. It is passed to the deserializer, which separates it into the original 11 data signals and the 2 CHANNEL_SEL lines that were input into the serializer on the bottomside. Another important output the serializer generates is the regenerated MCLK signal, which is the phase-locked replica of the bottomside clock.

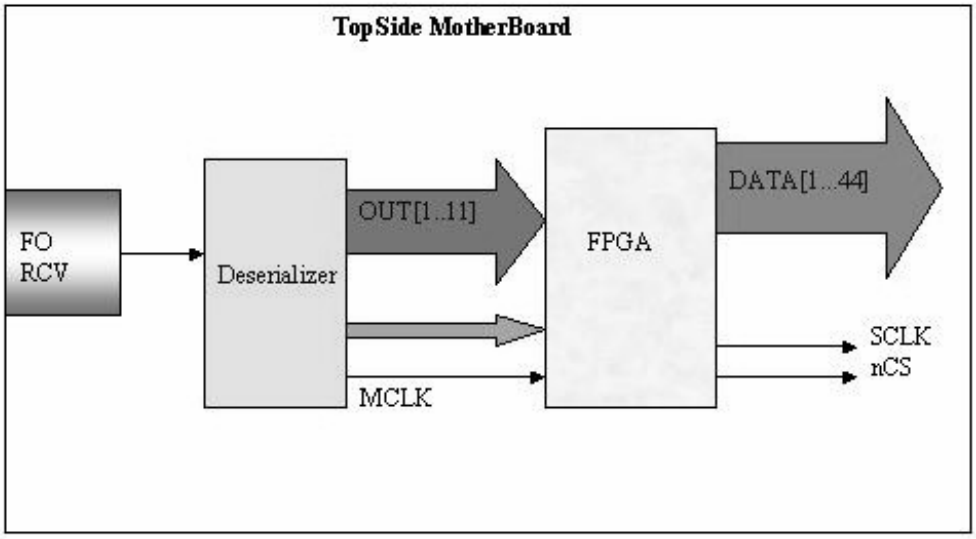

FIGURE 7. Topside Motherboard

The above outputs of the deserializer are passed to the FPGA. To retrieve the data, the process in the topside FPGA must be the reverse of the bottomside FPGA. To begin this process, four shift registers are created. Each shift register is 11 bits wide. The channel select lines that were passed from the deserializer are used to select the

corresponding shift register which corresponds to the same channel from the bottomside multiplexer. For example, in Fig. 8, when CHANNEL 1 goes high, it allows the contents of the data bus to load only Shift Reg #1 which is clocked in by the synchronous MCLK. This data corresponds to the original first 11 A/D channels, DATA[1..11].

Now that the original 44 digital data channels have been reconstructed, the digital data channels can be recorded in their present form or converted back to their original analog form using D/A converters. The D/A converter accepts 3 inputs which are the serial data, the sync bit, nCS, and the serial clock, SCLK. Both the nCS and SCLK are created inside the FPGA by the phase-locked replica of MCLK. Lastly, MCLK is divided down to 10 MHz to provide signal synchronization for topside acquisition and control.

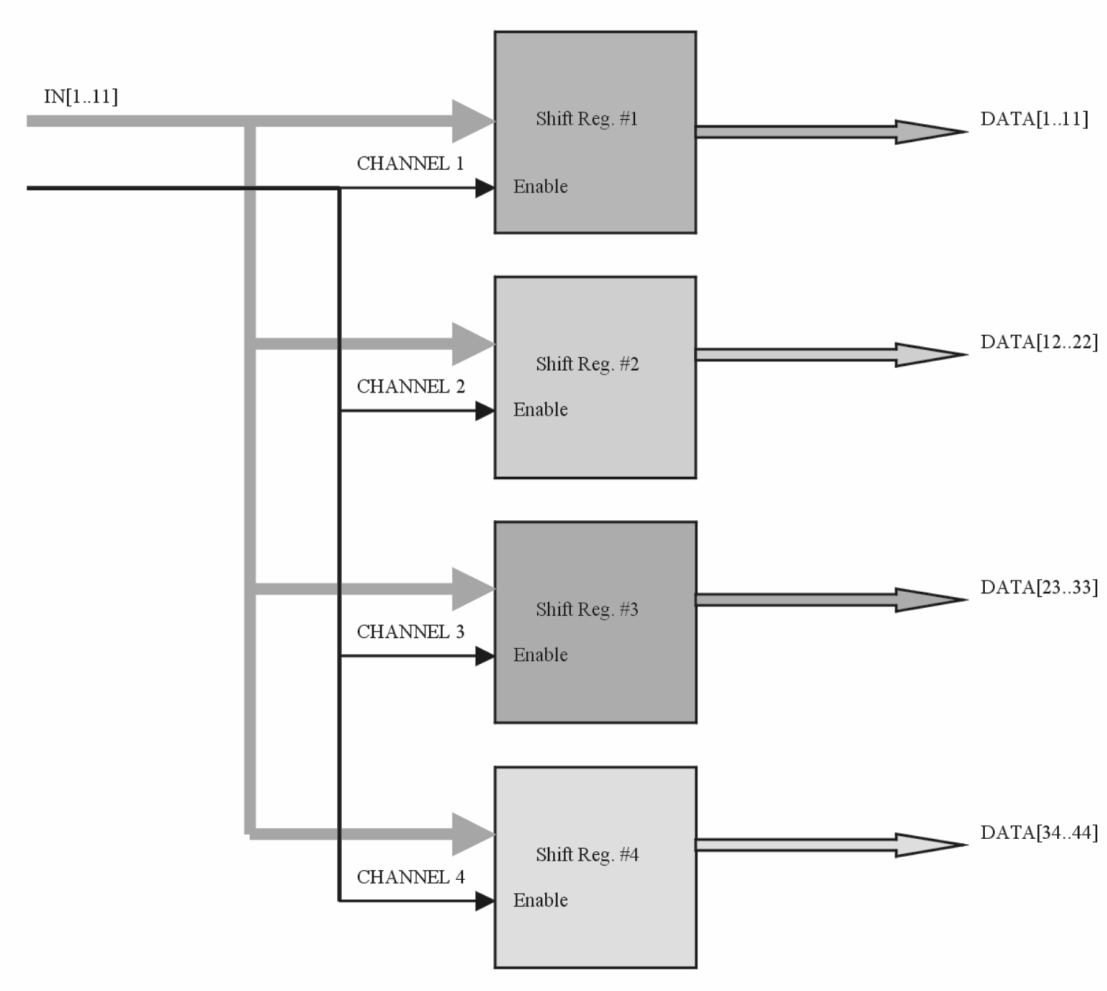

FIGURE 8. FPGA Demultiplexer

Topside Data Acquisition

The topside data acquisition system is shown in Figure 9. The signal received on each of the low and high-frequency acoustic arrays is bandpass filtered. For the high frequency data sets, the passband was 0.5 kHz – 200 kHz., and for the low-frequency data sets the passband was 0.5 kHz – 12 kHz. To insure that the system is phase locked to the topside data acquisition system, the sample clock and trigger are derived from the 10 MHz clock transmitted from the topside electronics which is phase-locked to the bottomside MCLK. Analog to digital conversion is accomplished using a CAMAC Crate configured with seven Joeger TR612/3 Transient recorders and a Fast CAMAC SCSI Crate controller. Each transient recorder is capable of simultaneous sampling six analog channels at a maximum sample rate of 3 MHz per channel. Each channel has 512 Mbytes of on board memory. Trigger and sample clocks are daisy chained across all seven recorders to insure that the conversion process is phase-locked. The digital data acquisition system is controlled using a PC with 3 GHz processor running Windows XP, and National Instruments LabView. The data was recorded on hard drive in real-time, and later archived to DVD's. Topside user interface software was designed to allow the operator to select which transient recorders are active and to monitor any of the active recorders. The capability to monitor the individual channels in real-time, allows the data acquisition trigger to be delayed until the received signal is completely contained within the digitized window.

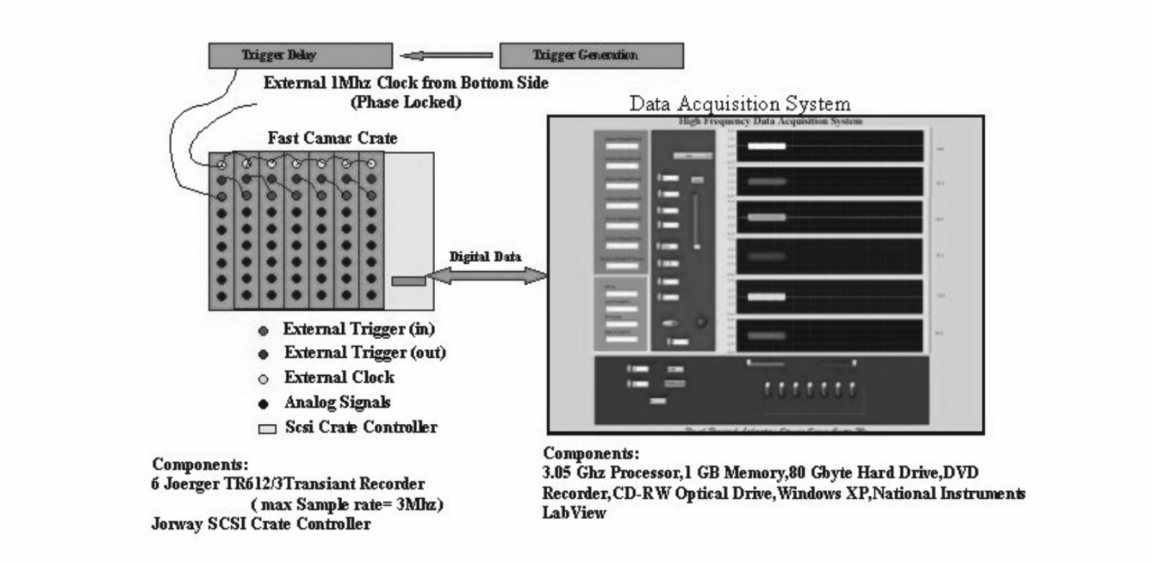

FIGURE 9. Analog Data Acquisition System

Summary

A multi-channel acquisition system was developed to support broadband coherence experiments that were performed in June 2003. Because of the technology used for the project, the system can be easily adapted with a minimal effort to support other future experiments and requirements.

ACKNOWLEDGMENTS

This work was supported by the Office of Naval Research, technical management by the Naval Research Laboratory under program element 62435N.

REFERENCES

1. Stanic, S.,et al., “Panama City 2003 broadband shallow-water acoustic coherence experiments,” in *Proceedings of the High-Fregquency Ocean Acoustics Conference*, 2004.
2. F. Xiong, *Digital Modulation Techniques* . Norwood, MA: Artech House Inc., 2000.
3. “DS92LV16 16-Bit Bus LVDS Serializer/Deserializer,” National Semiconductor Corporation, Santa Clara, Ca. 2001.